Verilog Course Team

10B.Chowdry Nagar Main Road,Valasaravakkam,Chennai-600087
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VLSI PROJECT TOPICS-2015

2003

- DCT-Based Image Watermarking Using Subsampling- Verilog with Matlab
- VLSI Implementation of Invisible Digital Watermarking Algorithms- Verilog with Matlab

2004

- An FPGA-based Architecture for Real Time Image Feature Extraction- Verilog with Matlab
- Contrast Enhancement of Color Images using Tunable Sigmoid Function- Verilog with Matlab
- Robust DWT-SVD Domain Image Watermarking Embedding Data in All Frequencies
- Shift Invert Coding (SINV) for Low Power VLSI
- VLSI Implementation of Discrete Wavelet Transform (DWT) and IDWT for Image Compression- Verilog with Matlab

2005

- A VLSI Architecture for Visible Watermarking in a Secure Still Digital Camera (S2DC) Design (Corrected)- Verilog with Matlab
- Digital Design of DS-CDMA Transmitter Using Verilog HDL and FPGA
- Visual Attention Driven Image to Video Adaptation- Verilog with Matlab

2006

- A Lossless Data Compression and Decompression Algorithm and Its Hardware Architecture
- A Verilog Implementation of UART Design with BIST Capability
- An Optimum ORA BIST for Multiple Fault FPGA Look-Up Table Testing
- Image Compression with Different Types of Wavelets- Verilog with Matlab

2007

- A Low-Power Multiplier With the Spurious Power Suppression Technique
- A VLSI architecture for a Run-time Multi-precision Reconfigurable Booth Multiplier
- Design and Implementation of a low complexity real lossless Image compression method for wireless endoscopy capture system- Verilog with Matlab
- Implementation of a Multi-channel UART Controller Based on FIFO Technique and FPGA
- Improvement of the Orthogonal Code Convolution Capabilities Using FPGA Implementation
- Low-power and high-quality Cordic-based Loeffler DCT for signal processing
- Low-Power Built-In Logic Block Observer Realization for BIST Applications-VHDL
- Video Adaptation for Small Display Based on Content Recomposition- Verilog with Matlab

- VLSI Implementation of High Speed and High Resolution FFT Algorithm Based on Radix 2 for DSP Application

2008

- A Robust UART Architecture Based on Recursive Running Sum Filter for Better Noise Performance
- FPGA Based Design of a Novel Enhanced Error Detection And Correction Technique
- FPGA Implementation of USB Transceiver Macrocell Interface with USB2.0 Specifications
- FPGA Implementation of a Scalable Encryption Algorithm
- Fuzzy based PID Controller using Verilog HDL for Transportation Application
- Implementation of 64 Point FFT using Vedic Multiplier
- Implementation of IEEE 802.11 a WLAN Baseband Processor
- Multiplier design based on ancient Indian vedic muliplier
- Research on Fast Super-resolution Image Reconstruction Base on Image Sequence-Verilog with Matlab
- VLSI Implementation of an Edge-Oriented Image Scaling Processor- Verilog with Matlab

2009

- 3D Discrete Wavelet Transform VLSI Architecture for Image Processing- Verilog with Matlab
- A Fast Hardware Approach for Approximate, Efficient Logarithm and Antilogarithm Computations
- An Effective Fast and Small-Area Parallel-Pipeline Architecture for OTM- Convolutional Encoders
- Biometric Encryption using Fingerprint Fuzzy Vault for FPGA-based Embedded Systems- Verilog with Matlab
- CSI Multimedia Architecture
- Fast Scaling in the Residue Number System
- Design and Implementation of Boundary-Scan Circuit
- FPGA Based Power Efficient Channelizer For Software Defined Radio
- FPGA-Based Face Detection System Using Haar Classifiers- Verilog with Matlab
- Hardware Algorithm for Variable Precision Multiplication on FPGA
- Implementing Gabor Filter for Fingerprint Recognition Using Verilog HDL- Verilog with Matlab
- VLSI Implementations of the Cryptographic Hash Functions MD6

2010

- FPGA Implementations of the Hummingbird Cryptographic Algorithm
- A High-speed 32-bit Signed Unsigned Pipelined Multiplier
- Software-Defined Radio for OFDM Transceivers
- VLSI Implementation of Fully Pipelined Multiplier less 2D DCT IDCT Architecture for JPEG- Verilog with Matlab
- Product Reed-Solomon Codes for Implementing NAND Flash Controller on FPGA chip

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- High Speed and Low Space Complexity FPGA Based ECC
- FPGA Implementation of Parallel 2-D MRI Image Filtering Algorithms- Verilog with Matlab
- FPGA Implementation of Modular Multiplication methods using Cellular Automata
- FPGA Implementation of High Performance LDPC Decoder using Modified 2-bit
- Design of Low-Power High-Speed Truncation-Error-Tolerant Adder
- Design of Low-Cost High-performance Floating-point Fused Multiply-Add with Reduced Power
- Coherent Amplitude Modulated QAM-QPSK
- A Pipeline VLSI Architecture for High-Speed Computation of the 1-D Discrete Wavelet Transform- Verilog with Matlab
- A New VLSI Architecture of Parallel Multiplier–Accumulator Based on Radix-2 Modified Booth Algorithm
- A Memory-Efficient and Highly Parallel Architecture for Variable Block Size Integer Motion Estimation in H.264AVC- Verilog with Matlab
- A High Performance Binary to BCD Converter for Decimal Multiplication.

2011

- A New Reversible Design of BCD Adder
- A Multichannel Watermarking DCT-DWT- Verilog with Matlab
- An Efficient Implementation of Floating Point Multiplier
- An implementation of a 2D FIR filter using the signed-digit number system- Verilog with Matlab
- Automatic Road Extraction using High Resolution Satellite Images based on Mean Shift Method- Verilog with Matlab
- Built-In Generation of Functional Broadside Tests Using a Fixed Hardware Structure
- Design and FPGA Implementation of CORDIC-based 8-point 1D DCT Processor
- Design and Implementation of APB Bridge based on AMBA 4.0
- Design and VLSI implementation of high-performance face-detection engine for mobile applications- Verilog with Matlab
- Design Enhancement of Combinational Neural Networks Using HDL based FPGA Framework for Pattern Recognition- Verilog with Matlab
- Efficient VLSI Architecture for Discrete Wavelet Transform- Verilog with Matlab
- FPGA based FFT Algorithm Implementation in WiMAX Communications System
- FPGA Implementation of an Adaptive Filter Robust to Impulsive Noise Two Approaches- Verilog with Matlab
- High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics
- Image Encryption Based On AES Key Expansion- Verilog with Matlab
- Parallel Architecture for Hierarchical Optical Flow Estimation Based on FPGA- Verilog with Matlab
- PCFICH Channel Design for LTE using FPGA- Verilog with Matlab
- Pipelined Architecture for FPGA Implementation of Lifting-Based DWT- Verilog with Matlab

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2012

- A Pipeline VLSI Architecture for Fast Computation of the 2-D Discrete Wavelet Transform- Verilog with Matlab
- A Region Merging Approach for Image Segmentation on FPGA- Verilog with Matlab
- An Efficient Viterbi Decoder
- Design of 64-bit low power parallel prefix VLSI adder for high speed arithmetic circuits
- Design of Low Power TPG Using LP-LFSR
- FPGA Based Real Time Face Detection using Adaboost and Histogram Equalization- Verilog with Matlab
- HDL Design for Image Segmentation using Gabor filter for Disease Detection- Verilog with Matlab
- High Speed and Area Efficient Vedic Multiplier
- High Speed Modified Booth Encoder Multiplier for Signed and Unsigned Numbers
- Improved Architectures for a Fused Floating-Point Add-Subtract Unit
- Low-Power and Area-Efficient Carry Select Adder
- Low-Power Variation-Aware Flip Flop
- Modified Architecture for Real-Time Face Detection using FPGA- VHDL with Matlab
- Very Low Resolution Face Recognition Problem- Verilog with Matlab
- Viterbi-Based Efficient Test Data Compression
- VLSI Architecture of Arithmetic Coder Used in SPIHT- Verilog with Matlab

2013

- Cordic for Fixed Angle Rotation
- Design and Implementation of 32 Bit Unsigned Multiplier Using CLAA and CSLA
- Design Of High Speed Floating Point Mac Using Vedic Multiplier And Parallel Prefix Adder
- Design of High Speed Low Power Multiplier using Reversible logic-a Vedic Mathematical Approach
- Design of High-speed low power Reversible Logic BCD Adder Using HNG gate
- Low-Power, High-Throughput, and Low-Area Adaptive FIR Filter Based on Distributed Arithmetic Techniques for Compensating Memory Errors in JPEG2000- Verilog with Matlab
- Visible and Infrared Image Fusion using the Lifting Wavelets- VHDL with Matlab
- VLSI Implementation of an Adaptive Edge -Enhanced Image Scalar for RealTime Multimedia Applications- Verilog with Matlab
- VLSI Implementation of an Adaptive Edge-Enhanced Color Interpolation Processor for Real-Time Video Applications- Verilog with Matlab

2014

- A Distributed Canny Edge Detector Algorithm and FPGA Implementation- Verilog with Matlab
- A New Secure Image Transmission Technique via Secret-Fragment-Visible Mosaic Images- Verilog with Matlab

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- Design and Implementation of Orthogonal Code Convolution Using Enhanced Error Control Technique
- FPGA Implementation of the C-Mantec Neural Network Constructive Algorithm
- High Speed Convolution and Deconvolution Algorithm (Based on Ancient Indian Vedic Mathematics)
- SW-HW Implementation of Image Covariance Descriptor For Person Detection Systems
- VLSI Based Image Zooming Application by a Novel Adaptive Edge Enhancement Technique- Verilog with Matlab
- Hardware Efficient VLSI Architecture for 3-D Discrete Wavelet Transform-Verilog with Matlab
- Area-Delay-Power Efficient Fixed-Point LMS Adaptive Filter With Low Adaptation-Delay-Verilog with Matlab
- ASIC Implementation of Two Stage Pipelined Multiplier
- Hardware Software Co-Simulation of Edge Detection for Image Processing System-Verilog with Matlab

2015

- Reviewing High-Radix Signed-Digit Adders
- A New-High Speed-Low Power-Carry Select adder Using Modified GDI
- Fully Pipelined Low-Cost and High-Quality Color Demosaicking VLSI Design for Real-Time Video Applications-Verilog HDL with Matlab
- A Modified Partial Product Generator for Redundant Binary Multipliers

The above listed topics are just for reference. If you have any new Ideas/Papers send to us at **info@verilogcourseteam.com** or Call **+91 98942 20795.**