VLSI PROJECT TOPICS-IEEE

Verilog Course Team-Chennai. www.verilogcourseteam.com

- Design of Delay-Insensitive Three Dimension Pipeline Array Multiplier for Image Processing-2002
- DCT-Based Image Watermarking Using Subsampling-2003
- Shift Invert Coding (SINV) for Low Power VLSI-2004
- Robust DWT-SVD Domain Image Watermarking: Embedding Data in All Frequencies-2004
- Digital Design of DS-CDMA Transmitter Using VHDL and FPGA-2005
- Design of Edge Detection Systems
- A VLSI Architecture for Visible Watermarking in a Secure Still Digital Camera (S2DC) Design (Corrected)-2005
- A Lossless Data Compression and Decompression Algorithm and Its Hardware Architecture-2006
- An FPGA-based Architecture for Real Time Image Feature Extraction-2004
- Image Compression with Different Types of Wavelets-2006

2007 Topics

- A VLSI architecture for a Run-time Multi-precision Reconfigurable Booth Multiplier Low-power and high-quality Cordic-based Loeffler DCT for signal processing
- Implementation of a Multi-channel UART Controller Based on FIFO Technique and FPGA
- A Low-Power Multiplier With the Spurious Power Suppression Technique
- FPGA Implementation(s) of a Scalable Encryption Algorithm
- VLSI Implementation of High Speed and High Resolution FFT Algorithm Based on Radix 2 for DSP Application

2008 Topics

- Fuzzy based PID Controller using VHDL for Transportation Application Research on Fast Super-resolution Image Reconstruction Base on Image Sequence
- A Robust UART Architecture Based on Recursive Running Sum Filter for Better Noise Performance
- FPGA Implementation Of Usb Transceiver Macrocell Interface With USB2.0 Specifications
- Multiplier design based on ancient Indian Vedic Mathematics
- A Symbol-Rate Timing Synchronization Method for Low Power Wireless OFDM Systems
- Design Exploration of a Spurious Power Suppression Technique (SPST) and Its Applications

- Implementation of IEEE 802.11 a WLAN Baseband Processor

2009 Topics

- The CSI Multimedia Architecture
- Design and Implementation of Boundary-Scan Circuit for FPGA
- Hardware Algorithm for Variable Precision Multiplication on FPGA
- VLSI Implementations of the Cryptographic Hash Functions MD6 and ïrRUPT
- VLSI Implementation of an Edge-Oriented Image Scaling Processor
- FPGA-Based Face Detection System Using Haar Classifiers
- An Effective Fast and Small-Area Parallel-Pipeline Architecture for OTM-Convolutional Encoders
- Fast Scaling in the Residue Number System
- VLSI Architecture and Chip for Combined Invisible Robust Watermarking
- Implementing Gabor Filter for Fingerprint Recognition Using Verilog HDL
- An Area-Efficient Universal Cryptography Processor for Smart Cards
- FPGA Based Power Efficient Channelizer for Software Defined Radio
- Improvement of the Orthogonal Code Convolution Capabilities Using FPGA Implementation
- Lossless Compression using Efficient Encoding of Bitmasks
- 3D Discrete Wavelet Transform VLSI Architecture for Image Processing
- A Fast Hardware Approach for Approximate, Efficient Logarithm and Antilogarithm Computations

2010 Topics

- Design of Low-Cost High-performance Floating-point Fused Multiply-Add with Reduced Power
- A High-speed 32-bit Signed/Unsigned Pipelined Multiplier
- A New VLSI Architecture of Parallel Multiplier–Accumulator Based on Radix-2 Modified Booth Algorithm
- FPGA Implementations of the Hummingbird Cryptographic Algorithm

VLSI PROJECT TOPICS-IEEE

Verilog Course Team-Chennai. www.verilogcourseteam.com

- FPGA Implementation(s) of a Scalable Encryption Algorithm
- A Memory-Efficient and Highly Parallel Architecture for Variable Block Size Integer Motion Estimation in H.264/AVC
- Contrast Enhancement of Color Images using Tunable Sigmoid Function
- Image Compression with Different Types of Wavelets
- Performance Efficient FPGA Implementation of Parallel 2-D MRI Image Filtering Algorithms using Xilinx System Generator.
- Design and FPGA Implementation of Modular Multiplication methods using Cellular Automata
- Image Edge Detection Based on FPGA
- VLSI Implementation of Autocorrelator and CORDIC algorithm for OFDM based WLAN
- Improvisation of Gabor Filter design using Verilog HDL
- Product Reed-Solomon Codes for Implementing NAND Flash Controller on FPGA chip
- A Pipeline VLSI Architecture for High-Speed Computation of the 1-D Discrete Wavelet Transform
- VLSI Implementation of Fully Pipelined Multiplierless 2D DCT/IDCT Architecture for JPEG

2011 Topics

- An Efficient Implementation of Floating Point Multiplier
- High Speed and Low Space Complexity FPGA Based ECC Processor
- A blind digital watermarking algorithm based on wavelet transform
- A Distributed Canny Edge Detector And Its Implementation on FPGA
- Design and Simulation of UART Serial Communication Module Based on VHDL
- Design and VLSI implementation of high-performance face-detection engine for mobile applications
- Design and Implementation of Area-optimized AES based on FPGA
- Design of Low Power And High Speed Configurable Booth Multiplier
- Face detection and recognition method based on skin color and depth information
- High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics
- A New Reversible Design of BCD Adder

VLSI PROJECT TOPICS-IEEE

Verilog Course Team-Chennai. www.verilogcourseteam.com

- Digital Image Authentication from JPEG Headers
- Design and Implementation of Low Power Digital FIR Filter based on low power multipliers and adders on xilinx FPGA
- Parallel Architecture for Hierarchical Optical Flow Estimation Based on FPGA
- A Very Fast and Low Power Carry Select Adder Circuit
- A_multichannel watermaking scheme based on DCT-DWT
- An Implementation of a 2D FIR Filter Using the Signed-Digit Number System
- Design and Characterization of Parallel Prefix Adders using FPGAs
- FPGA based FFT Algorithm Implementation in WiMAX Communications System
- FPGA Design of AES Core Architecture for Portable Hard Disk
- FPGA Implementation of RS232 to Universal serial bus converter
- Image Encryption Based On AES Key Expansion
- Feature Extraction of Digital Aerial Images by FPGA based implementation of edge detection algorithms
- An Efficient Architecture Design for VGA Monitor Controller
- Curve Fitting Algorithm FPGA implementation
- FPGA Implementation of AES Algorithm
- Design of Low Power Column Bypass Multiplier using FPGA
- Design of Serial Communication Interface Based on FPGA
- Design and Implementation of an FPGA-based Real-Time Face Recognition System
- VHDL Design and FPGA Implementation of Weighted Majority Logic Decoders
- Low Cost Binary128 Floating-Point FMA Unit Design with SIMD Support
- Design of Low Power And High Speed Configurable Booth Multiplier
- Design Enhancement Of combinational Neural Networks using HDL Based FPGA framework for Pattern Recognition
- Efficient VLSI Architecture for Discrete Wavelet Transform

2012 Topics

- Design of 64-Bit Low Power Parallel Prefix VLSI Adder for High Speed Arithmetic Circuits
- DESIGN OF LOW POWER HIGH SPEED VLSI ADDER SUBSYSTEM

VLSI PROJECT TOPICS-IEEE

Verilog Course Team-Chennai. www.verilogcourseteam.com

- Synthesis and Implementation of UART using VHDL Codes
- HICPA: A Hybrid Low Power Adder for High-Performance Processors
- Low-Power and Area-Efficient Carry Select Adder
- Design and Implementation of Two Variable Multiplier Using KCM and Vedic Mathematics
- Design and Implementation of a High Performance Multiplier using HDL
- DESIGN Of LOW-POWER AND HIGH PERFORMANCE RADIX-4 MULTIPLIER
- Design of Plural-Multiplier Based on CORDIC Algorithm for FFT Application
- FPGA implementation of Binary Coded Decimal Digit Adders and Multipliers
- High Speed and Area Efficient Vedic Multiplier
- High speed Modified Booth Encoder multiplier for signed and unsigned numbers
- An Efficient VLSI Architecture for Lifting-Based Discrete Wavelet Transform
- High Speed Signed Multiplier for Digital Signal Processing Applications
- Accumulator Based 3-Weight Pattern Generation
- Design of Low Power TPG Using LP-LFSR
- Viterbi-Based Efficient Test Data Compression
- A Feature-Based Robust Digital Image Watermarking Scheme
- Digital Image Watermarking Based on Super Resolution Image Reconstruction
- Hardware Implementation of a Digital Watermarking System for Video Authentication
- Watermarking Mobile Phone Colour Images with Reed Solomon Error Correction Code
- Watermarking Scheme for Copyright Protection of 3d Animated Model
- Efficiency of BCH Codes in Digital Image Watermarking
- Image Magnification by Modifying DCT Coefficients
- A Real-time Face Detection And Recognition System
- VHDL Implementation of UART with Status Register
- Implementation of Hybrid Wave-pipelined 2D DWT Using ASIC
- FPGA Based Real Time Face Detection using Adaboost and Histogram Equalization
- Pipelined Parallel FFT Architectures via Folding Transformation

VLSI PROJECT TOPICS-IEEE

Verilog Course Team-Chennai. www.verilogcourseteam.com

- VHDL Design for Image Segmentation using Gabor filter for Disease Detection.
- AN EFFICIENT VITERBI DECODER
- Improved Architectures for a Fused Floating-Point Add-Subtract Unit
- Very Low Resolution Face Recognition Problem
- Improved Architectures for a Fused Floating-Point Add-Subtract Unit
- Area-Efficient VLSI Implementation for Parallel Linear-Phase FIR Digital Filters of Odd Length Based on Fast FIR Algorithm

The above listed topics are just for reference. If you have any new Ideas/Papers send to us at info@verilogcourseteam.com or Call +91 98942 20795.