VLSI TRAINING MODULES

Module: 1 -Digital Systems

- Boolean Algebra
- Combinational /Sequential Circuits
- K-Map Simplification
- Flip flop and Latches
- State Machines
- Counters and Shift Registers
- Case Studies

Module: 2 –Verilog HDL Programming

- Introduction to HDL
- Verilog Modeling Concepts
- Verilog HDL Conventions
- Data Types in Verilog
- Gate Level Modeling
- Operators
- Continuous Assignments
- Behavioral Modeling
- Compiler Directives
- Tasks and Functions
- Test benches-Basics
- Assignments
- Writing Verilog Models

Module: 3 –VHDL Programming

- Introduction
- Levels of representation and abstraction
- Basic Structure of a VHDL file
    - Behavioral model
    - Concurrency
    - Structural description
- Lexical Elements of VHDL
- Data Objects: Signals, Variables and Constants
    - Variable
    - Signal
    - Data Types
- Interger types
    - Attributes
- Operators
- Behavioral Modeling: Sequential Statements
    - Looping statement
    - Dataflow Modeling – Concurrent Statements
- Structural Modeling
- Data Flow Modeling

Module: 4 –System Verilog

- Introduction
    - History of Verilog HDL
    - What is SystemVerilog

- SystemVerilog Verification Environment

- Language Overview
  - 2001 structures
  - Data types
  - Array
  - Struct/union
  - Module and interface
  - Operators
  - Event scheduling in System Verilog Program
- SystemVerilog Classes
- Random Constraints
- SystemVerilog Assertions
- Functional Coverage
- System Tasks And Functions
- VMM Tutorial
- OVM Tutorial

Module: 5 –FPGA Synthesis

- Working Process with Synthesis tool
- Setting Constraints
- Timing Analysis-Introduction

Module: 6- FPGA Implementation

- Implementation Procedures
- Setting Target Device
- Device Programming using ALTERA/XILINX

Module: 7 –ASIC Synthesis

- ASIC Synthesis-Materials
- Working Process with Synthesis tool
- Setting Technology-libraries
- Setting Constraints
- Introduction to Shell and TCL scripting.

Module: 8- EDA Simulation Tools

- Mentor Graphics- Modelsim/Questasim
- Synopsys - VCS
- Cadence - NC Verilog/Verilog XL

Module: 9- EDA Synthesis Tools

- Xilinx - Xilinx ISE (FPGA)
- Altera -Quartus II (FPGA)
- Synopsys - Design Complier (ASIC)

Module: 10- Operating Systems

- Red Hat
- Windows
- Sun Solaris

VLSI TRAINING MODULES

Module: 11 - Project Planning/Management

- Design Specification Analysis
- Directory Structure
- Test Plan
- Test Environment
- RTL-Coding Guidelines
- Documentation

Module: 12 – Real Time- Industry Standard Project

- AMBA
- PCI EXPRESS
- USB