Introduction to

PCI Express

By

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The motivation is to give the reader an easy to follow, introductory overview of PCI Express architecture. We hope that this document is easy to read and understandable format.

Feel free to give your feedback/suggestion to improve the tutorial in-depth.

INTRODUCTION

When look back to history we can find so many advancement in technology day today life. When refer to the technology, can find lot of development between every stage. In communication and computer sector the growth is drastic change, people can communicate any where in the world in few seconds because of technical advancement. There are certain times in the evolution of Technology for every generation. Because of technology revolution a new input/output architecture, PCI Express allows computer to process far beyond the limit when compared with the existing technology. The term PCI - Peripheral Component Interconnect.PCI Express is the third generation I/O interconnects.PCI Express communicate the devices simultaneously by implementing dual unidirectional paths, this makes the protocol high speed and low voltage.

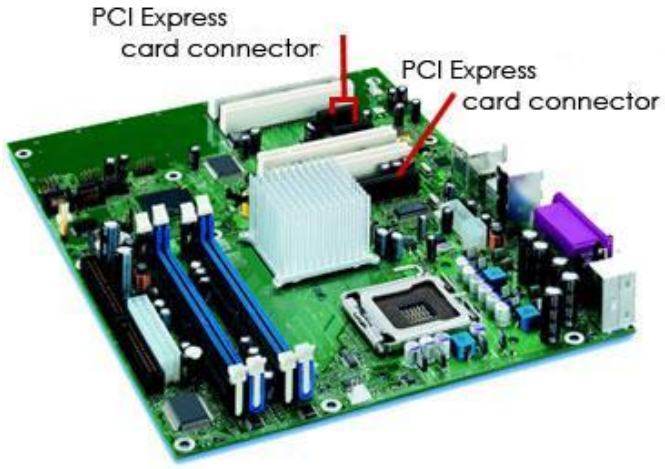

Figure: 1 PCI Express Card Connector Model

The three main technologies,

- PCI
- PCI- X (Derivative of PCI)
- PCI- Express

PCI-X is not the abbreviation of PCI Express. PCI-X evolved from PCI.

PCI-Express

The major difference between PCI Express and PCI, PCI-Express is a Serial Point to Point interface, whereas PCI is a Parallel. A PCI-Express device is always the driver for its transmitter pairs(s) and is always the target for its receiver pair(s).The Connection between two PCI Express devices is referred to as Link. A links consist of number of Lanes. A lane is a combination of Transmit and Receive pairs. For the first generation of PCI Express technology, there is only one signaling rate defined, which provides an effective 2.5 Gigabits/second/Lane/direction of raw bandwidth. The data rate is expected to increase with technology advances in the future.

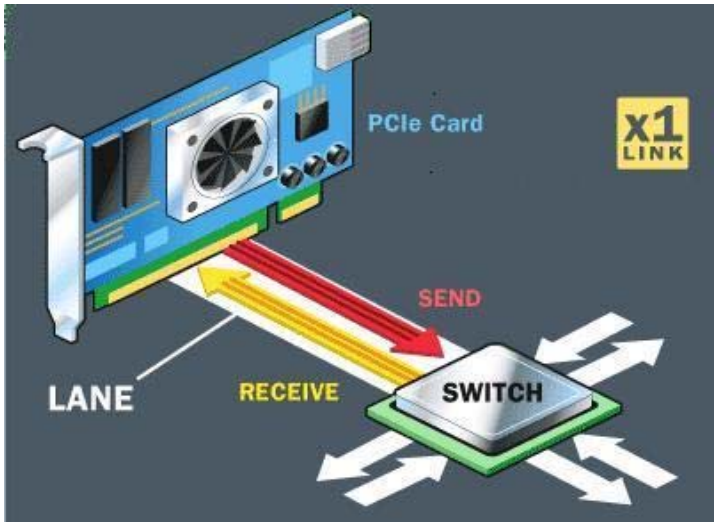

Figure: 2 PCI Express X1 Link Model

PCI Express configuration has serial links: X1, X2, X4, X8, X12, X16 and X32. An X1 configuration has a single serial path of Transmit and Receive. Likewise X2 configurations have two serial paths of Transmit and Receive. The serial links pronounced as or read as ” by one “- X1 and “by two”-X2 and so on.

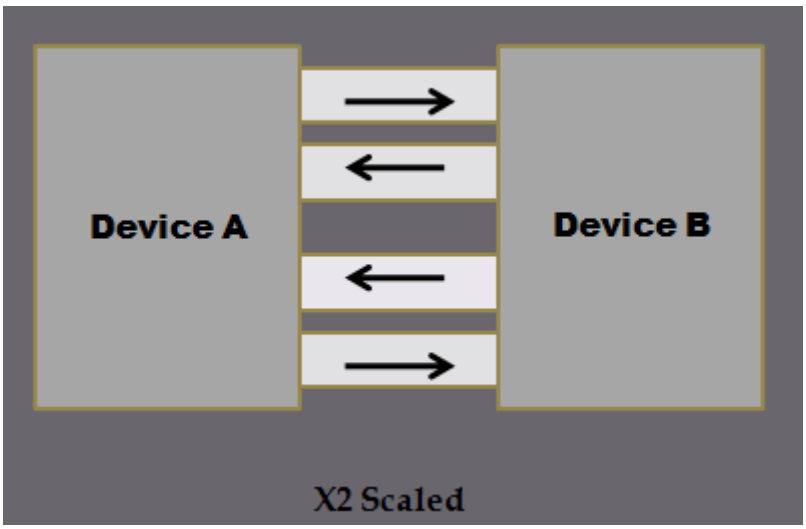

Figure: 3 Model of X2 serial links

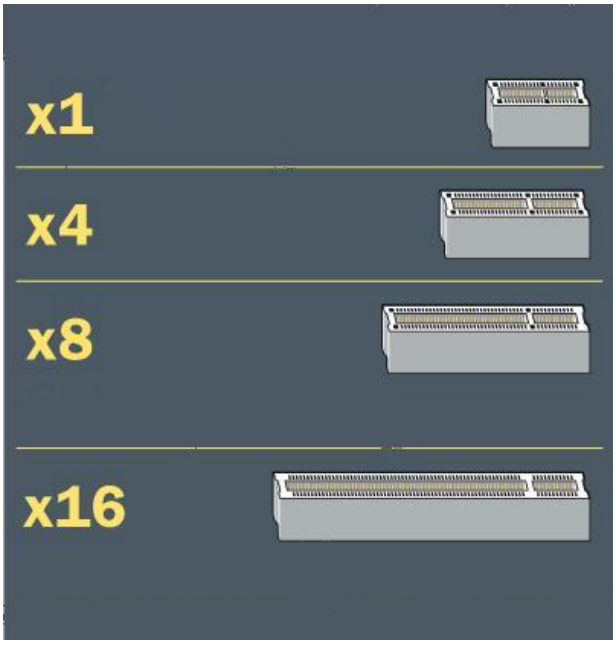

Figure: 4 PCI Express Connector Models X1, X4, X8, X16

PCI Express Layering Overview

As shown in the figure: 5, PCI Express has three discrete logical layers:

- Transaction Layer
- Data Link Layer
- Physical Layer

Each of these layers is divided into two sections: Transmit and Receive block.

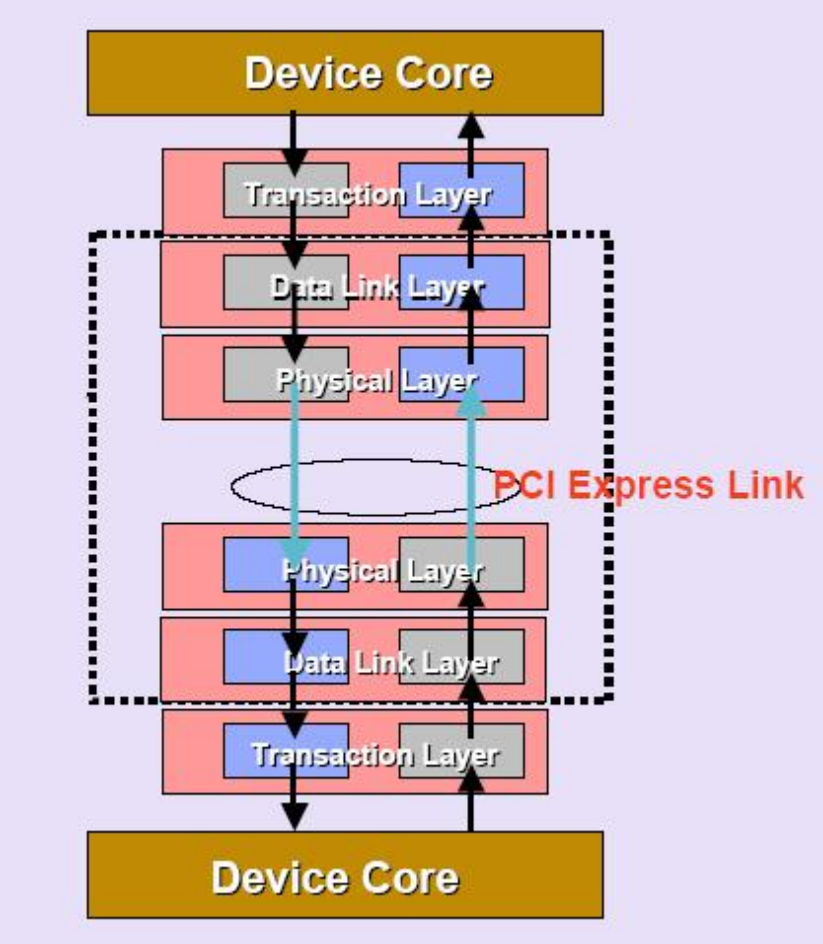

Figure: 5 PCI Express Layering Diagram Model

TRANSACTION LAYER

The Upper Layer of the architecture is the Transaction Layer. The main responsible of this layer is to begin the process of turning request or completion from device core into PCI Express transactions.

On the Transmit side, the transaction layer receives request or completion data from the core, and turns that information into out going PCI Express transaction.

On the Receive side the transaction layer accepts the incoming PCI Express transactions from its Data Link Layer.

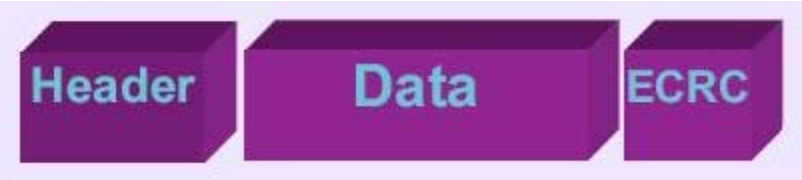

Figure: 6 Transaction Layer Model

Transaction Layer uses TLP-Transaction Layer Packet to communicate request and complete data into other PCI Express devices. Each TLP has a Header to identify the type of transaction. The Transaction Layer request device generates the TLP and completion device consumes the TLP. Transaction Layer has several other operations which include “Flow Control” and “Power Management”.

Header identifies the information for the transaction (types). PCI Express architecture defines four transaction types.

- Memory Transaction
- I/O Transaction

- Configuration Transaction
- Message Transaction

Where as DLP and ECRC (End to End CRC) are optional.

DATA LINK LAYER

The Data Link Layer acts as an intermediate Layer between Transaction and Physical Layer, nothing but a Gate Keeper. The main responsibility of Data Link Layer is Error detection and correction.

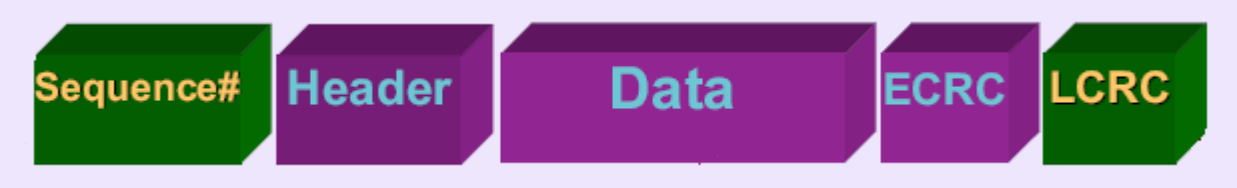

Figure: 7 Data Link Layer Model

Data Link Layer takes the TLP-Transaction Layer Packet from transmit side of the Transaction Layer. Here 12 bit sequence Number is added in front of the TLP and LCRC-Link CRC checker to the end.

Data Link Layer then forwards the applied TLP to the Physical Layer transmit side. On the receive side of Data Link Layer, accepts the packet from Physical Layer and checks the Sequence Number and LCRC with the applied Sequence Number and LCRC. If the Sequence Number/LCRC matches then the TLP are moved to receive side of Transaction Layer and generates ACK (Acknowledgement) signal. If there is any mismatches/error detects in Sequence Number or LCRC then Data Link Layer does not send the “Invalid or

Bad" TLP to receive side of Transaction Layer, instead it generates NAK (Negative Acknowledgement). Data Link Layer now starts "Retry" attempts to send the valid TLP to Transaction Layer.

PHYSICAL LAYER

The lowest layer of PCI Express is the Physical Layer. The main responsibility of this layer is sending and receiving of all data across the PCI Express link.

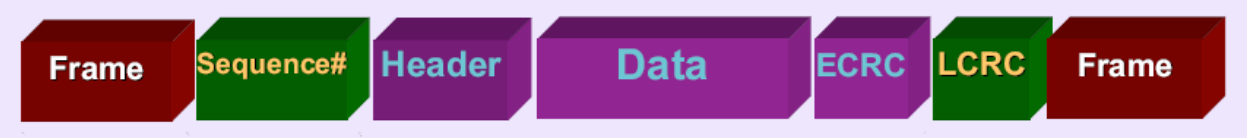

Figure: 8 Physical Layer Model

On the transmit side of Physical Layer the information taken from Data Link Layer and converts the parallel data into serial data format, nothing but a parallel to serial conversion. In additional framing characters is added to indicate the starting and ending of the packet.

On the receive side of Physical Layer the incoming serial data from PCI Express link is converted into its original format such that parallel data and the added frames are removed and the packets are send back to Data Link Layer.