Verilog/Digital FAQS

By

Verilog Course Team

Email:info@verilogcourseteam.com

www.vlsi-faqs.blogspot.com

www.verilogcourseteam.com

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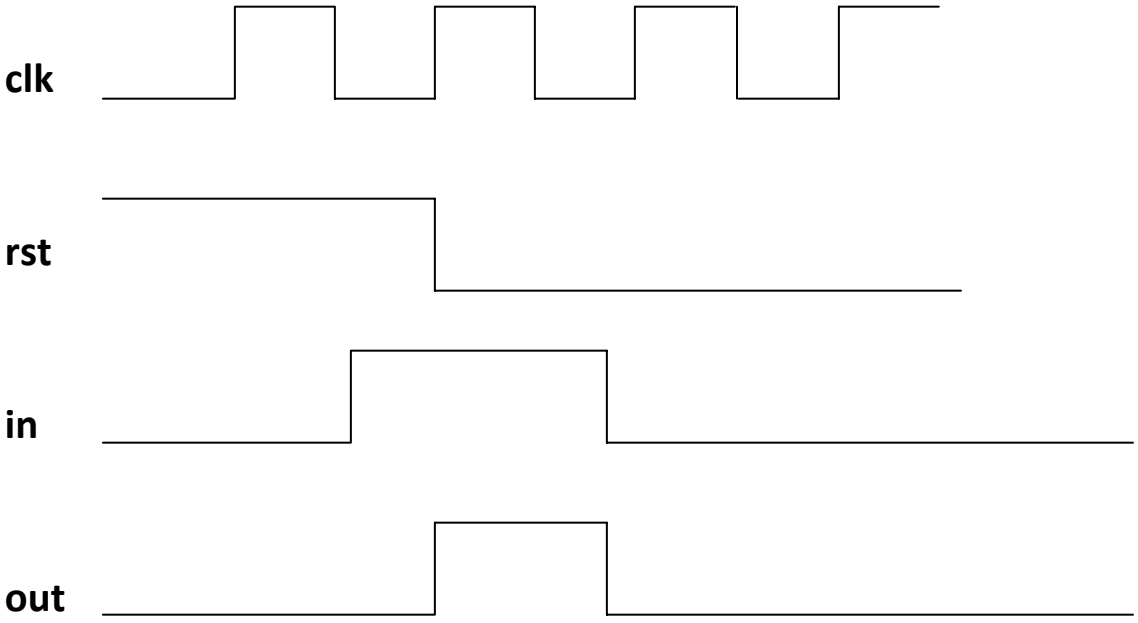
Our mission is to provide cost effective, technology independent, good quality reusable Intellectual Property cores with quality and cost factor are our important constraints so as to satisfy our customers ultimately. We develop and continuously evaluate systems so as to pursue quality in all our deliverables. At our team, we are completely dedicated to customer's requirements. Our products are designed and devoted to empower their competitive edge and help them succeed.

1.Design a circuit(positive edge) that detect the sequence when input changes from 0 to 1,the output should go high for only one clock pulse.



2. Design a circuit to detect when the 2-16 bits inputs are same.

3. Assume b = 3 and c = 5, after the first @ (posedge clk) what is the value of a?

```
always @ (posedge clk)
        a = b;

always @ (posedge clk)
        b = c;
```

4. After the first @ (posedge clk), does this do a swap?

```
always @ (posedge clk)
 begin
        a = b;
        b = a;
 end
```

5. Consider the following code:

```
`define FALSE 0
`define TRUE 1
initial
  begin
a = `FALSE;
a <= `TRUE;
if (a == `TRUE)
$display ("True");
else
$display ("False");
 end
```

What will print out? True or False?

6. Design AND, OR gate using 2:1 mux.

7. Draw the circuit to avoid the Set-up and Hold-time violation.

8. Consider the following code:

```
always@(posedge clk)
if(rst==0)
out<=1'b0;
else
out<=data_in;
```

a. Draw the synthesis view for the above code.
b. Modify the code for Asynchronous Reset.
c. Draw the timing diagram for synchronous and asynchronous reset.

9. How to test the functionality (test cases) of a FIFO.

10. What is the advantage of using Gray code instead of Binary code while designing FIFO.

11. What are the parameters to be considered before starting the design work.

12. Design EX-OR gate using 4 NAND gates.

13. Design EX-NOR gate using 4 NOR gates.

14. What will be the synthesis structure?

```
module two_stage(Q, D, CLK);
input D, CLK;
output Q;

reg Q, P;

always @ (posedge CLK)
  begin
     Q = P;
     P = D;
 end
```

```
module two_stage(Q, D, CLK);
input D, CLK;
output Q;

reg Q, P;

always @ (posedge CLK)
  begin
     Q <= P;
     P <= D;
 end
```

```
module two_stage(Q, D, CLK);
input D, CLK;
output Q;

reg Q, P;

always @ (posedge CLK)
  begin
     P = D;
     Q = P;
end
```

```
module two_stage(Q, D, CLK);
input D, CLK;
output Q;

reg Q, P;

always @ (posedge CLK)
  begin
     P <= D;
     Q <= P;
end
```

15. Consider the following code,

```
always@(posedge clk)
 begin
      a=b;
      b=c;
      c=a;
end
```

What logic does the code implies.